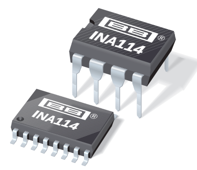
BURR - BROWN®




# INA114

# Precision INSTRUMENTATION AMPLIFIER

## FEATURES

- LOW OFFSET VOLTAGE: 50µV max
- LOW DRIFT: 0.25µV/°C max
- LOW INPUT BIAS CURRENT: 2nA max
- HIGH COMMON-MODE REJECTION: 115dB min
- INPUT OVER-VOLTAGE PROTECTION: ±40V
- WIDE SUPPLY RANGE: ±2.25 to ±18V
- LOW QUIESCENT CURRENT: 3mA max
- 8-PIN PLASTIC AND SOL-16

## APPLICATIONS

- BRIDGE AMPLIFIER
- THERMOCOUPLE AMPLIFIER
- RTD SENSOR AMPLIFIER
- MEDICAL INSTRUMENTATION
- DATA ACQUISITION

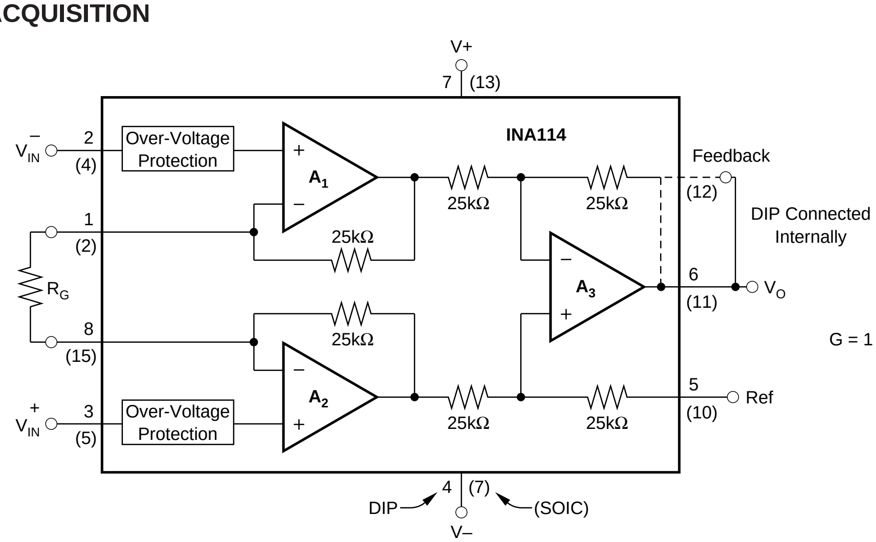
## DESCRIPTION

The INA114 is a low cost, general purpose instrumentation amplifier offering excellent accuracy. Its versatile 3-op amp design and small size make it ideal for a wide range of applications.

A single external resistor sets any gain from 1 to 10,000. Internal input protection can withstand up to ±40V without damage.

The INA114 is laser trimmed for very low offset voltage (50µV), drift (0.25µV/°C) and high common-mode rejection (115dB at G = 1000). It operates with power supplies as low as ±2.25V, allowing use in battery operated and single 5V supply systems. Quiescent current is 3mA maximum.

The INA114 is available in 8-pin plastic and SOL-16 surface-mount packages. Both are specified for the –40°C to +85°C temperature range.




$$G = 1 + \frac{50k\Omega}{R_G}$$


International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111 • Twx: 910-952-1111
Internet: http://www.burr-brown.com/ • FAXLine: (800) 548-6133 (US/Canada Only) • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132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# SPECIFICATIONS

## ELECTRICAL

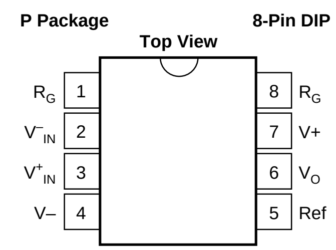
At $T_A$ = +25°C, $V_S$ = ±15V, $R_L$ = 2kΩ, unless otherwise noted.

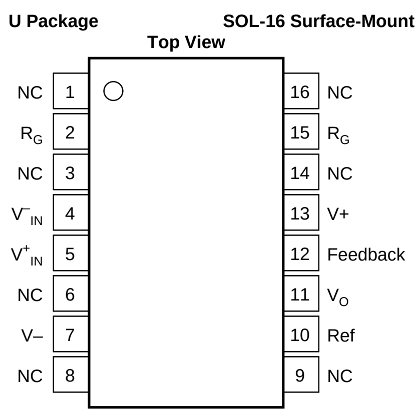
| PARAMETER | CONDITIONS | INA114BP, BU MIN | INA114BP, BU TYP | INA114BP, BU MAX | INA114AP, AU MIN | INA114AP, AU TYP | INA114AP, AU MAX | UNITS |
|---|---|---|---|---|---|---|---|---|
| **INPUT** | | | | | | | | |
| Offset Voltage, RTI | | | | | | | | |
| Initial | $T_A$ = +25°C | | ±10 + 20/G | ±50 + 100/G | | ±25 + 30/G | ±125 + 500/G | μV |
| vs Temperature | $T_A$ = $T_{MIN}$ to $T_{MAX}$ | | ±0.1 + 0.5/G | ±0.25 + 5/G | | ±0.25 + 5/G | ±1 + 10/G | μV/°C |
| vs Power Supply | $V_S$ = ±2.25V to ±18V | | 0.5 + 2/G | 3 + 10/G | | * | * | μV/V |
| Long-Term Stability | | | ±0.2 + 0.5/G | | | * | | μV/mo |
| Impedance, Differential | | | $10^{10} \parallel 6$ | | | * | | Ω ∥ pF |
| Common-Mode | | | $10^{10} \parallel 6$ | | | * | | Ω ∥ pF |
| Input Common-Mode Range | | ±11 | ±13.5 | | * | * | | V |
| Safe Input Voltage | | | | ±40 | | | * | V |
| Common-Mode Rejection | $V_{CM}$ = ±10V, $\Delta R_S$ = 1kΩ | | | | | | | |
| | G = 1 | 80 | 96 | | 75 | 90 | | dB |
| | G = 10 | 96 | 115 | | 90 | 106 | | dB |
| | G = 100 | 110 | 120 | | 106 | 110 | | dB |
| | G = 1000 | 115 | 120 | | 106 | 110 | | dB |
| **BIAS CURRENT** | | | ±0.5 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| **OFFSET CURRENT** | | | ±0.5 | ±2 | | * | ±5 | nA |
| vs Temperature | | | ±8 | | | * | | pA/°C |
| **NOISE VOLTAGE, RTI** | G = 1000, $R_S$ = 0Ω | | | | | | | |
| f = 10Hz | | | 15 | | | * | | nV/√Hz |
| f = 100Hz | | | 11 | | | * | | nV/√Hz |
| f = 1kHz | | | 11 | | | * | | nV/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 0.4 | | | * | | μVp-p |
| Noise Current | | | | | | | | |
| f=10Hz | | | 0.4 | | | * | | pA/√Hz |
| f=1kHz | | | 0.2 | | | * | | pA/√Hz |
| $f_B$ = 0.1Hz to 10Hz | | | 18 | | | * | | pAp-p |
| **GAIN** | | | | | | | | |
| Gain Equation | | | 1 + (50kΩ/$R_G$) | | | * | | V/V |
| Range of Gain | | 1 | | 10000 | * | | * | V/V |
| Gain Error | G = 1 | | ±0.01 | ±0.05 | | * | * | % |
| | G = 10 | | ±0.02 | ±0.4 | | * | ±0.5 | % |
| | G = 100 | | ±0.05 | ±0.5 | | * | ±0.7 | % |
| | G = 1000 | | ±0.5 | ±1 | | * | ±2 | % |
| Gain vs Temperature | G = 1 | | ±2 | ±10 | | * | ±10 | ppm/°C |
| 50kΩ Resistance(1) | | | ±25 | ±100 | | * | * | ppm/°C |
| Nonlinearity | G = 1 | | ±0.0001 | ±0.001 | | * | ±0.002 | % of FSR |
| | G = 10 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G = 100 | | ±0.0005 | ±0.002 | | * | ±0.004 | % of FSR |
| | G = 1000 | | ±0.002 | ±0.01 | | * | ±0.02 | % of FSR |
| **OUTPUT** | | | | | | | | |
| Voltage | $I_O$ = 5mA, $T_{MIN}$ to $T_{MAX}$ | ±13.5 | ±13.7 | | * | * | | V |
| | $V_S$ = ±11.4V, $R_L$ = 2kΩ | ±10 | ±10.5 | | * | * | | V |
| | $V_S$ = ±2.25V, $R_L$ = 2kΩ | ±1 | ±1.5 | | * | * | | V |
| Load Capacitance Stability | | | 1000 | | | * | | pF |
| Short Circuit Current | | | +20/–15 | | | * | | mA |
| **FREQUENCY RESPONSE** | | | | | | | | |
| Bandwidth, –3dB | G = 1 | | 1 | | | * | | MHz |
| | G = 10 | | 100 | | | * | | kHz |
| | G = 100 | | 10 | | | * | | kHz |
| | G = 1000 | | 1 | | | * | | kHz |
| Slew Rate | $V_O$ = ±10V, G = 10 | 0.3 | 0.6 | | * | * | | V/μs |
| Settling Time, 0.01% | G = 1 | | 18 | | | * | | μs |
| | G = 10 | | 20 | | | * | | μs |
| | G = 100 | | 120 | | | * | | μs |
| | G = 1000 | | 1100 | | | * | | μs |
| Overload Recovery | 50% Overdrive | | 20 | | | * | | μs |
| **POWER SUPPLY** | | | | | | | | |
| Voltage Range | | ±2.25 | ±15 | ±18 | * | * | * | V |
| Current | $V_{IN}$ = 0V | | ±2.2 | ±3 | | * | * | mA |
| **TEMPERATURE RANGE** | | | | | | | | |
| Specification | | –40 | | 85 | * | | * | °C |
| Operating | | –40 | | 125 | * | | * | °C |
| $\theta_{JA}$ | | | 80 | | | * | | °C/W |

* Specification same as INA114BP/BU.

NOTE: (1) Temperature coefficient of the "50kΩ" term in the gain equation.

## PIN CONFIGURATIONS




## ABSOLUTE MAXIMUM RATINGS(1)

| | |
|---|---|
| Supply Voltage | ±18V |
| Input Voltage Range | ±40V |
| Output Short-Circuit (to ground) | Continuous |
| Operating Temperature | –40°C to +125°C |
| Storage Temperature | –40°C to +125°C |
| Junction Temperature | +150°C |
| Lead Temperature (soldering, 10s) | +300°C |

NOTE: (1) Stresses above these ratings may cause permanent damage.

# ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

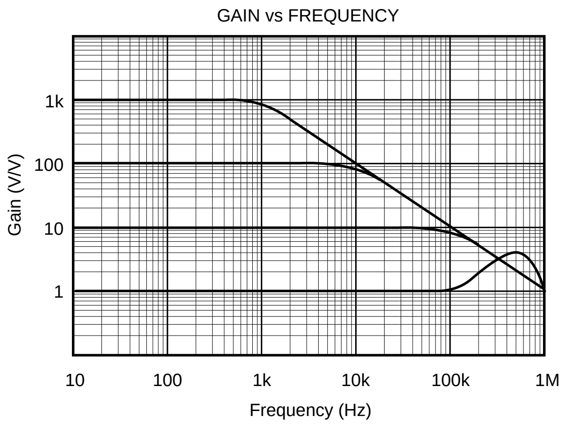
## PACKAGE/ORDERING INFORMATION

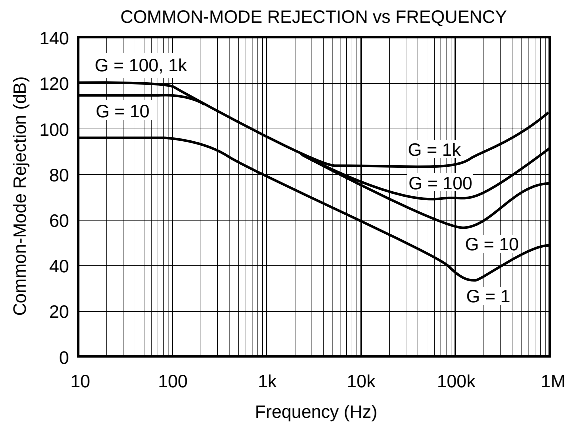
| PRODUCT | PACKAGE | PACKAGE DRAWING NUMBER(1) | TEMPERATURE RANGE |
|---|---|---|---|
| INA114AP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA114BP | 8-Pin Plastic DIP | 006 | –40°C to +85°C |
| INA114AU | SOL-16 Surface-Mount | 211 | –40°C to +85°C |
| INA114BU | SOL-16 Surface-Mount | 211 | –40°C to +85°C |

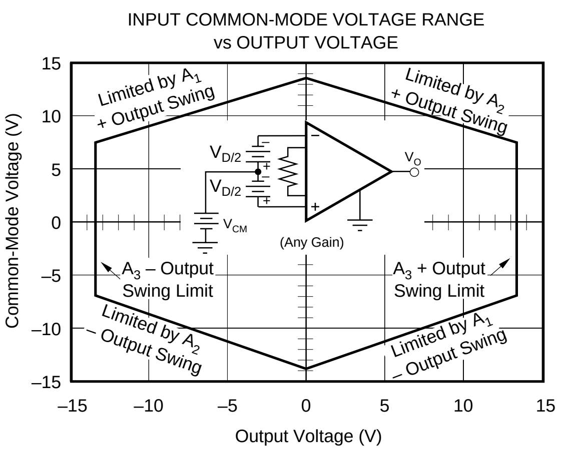
NOTE: (1) For detailed drawing and dimension table, please see end of data sheet, or Appendix C of Burr-Brown IC Data Book.

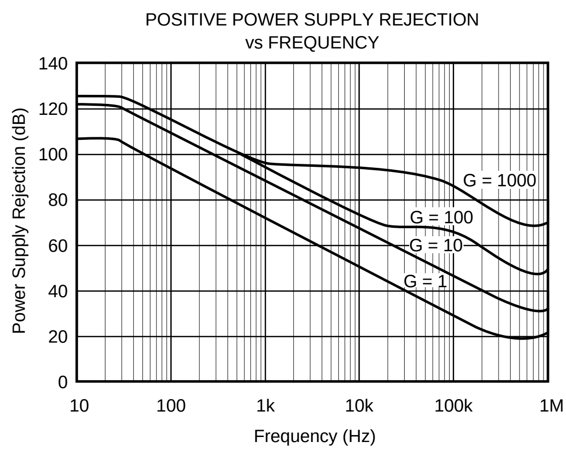
# TYPICAL PERFORMANCE CURVES

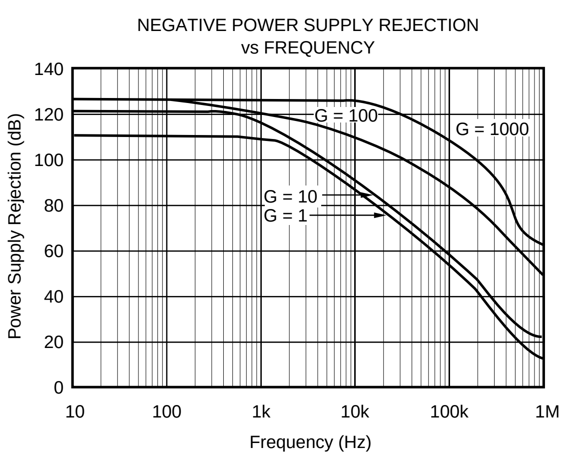
At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

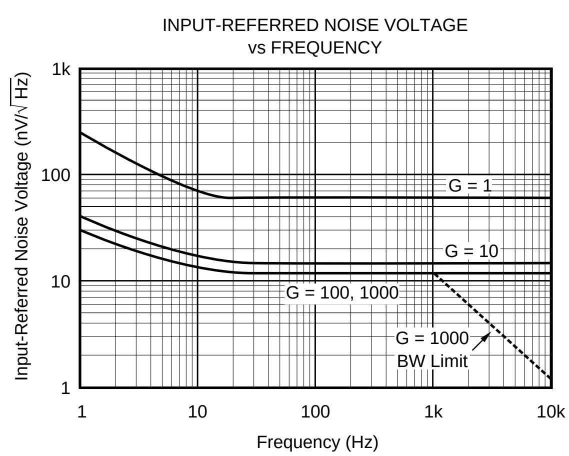


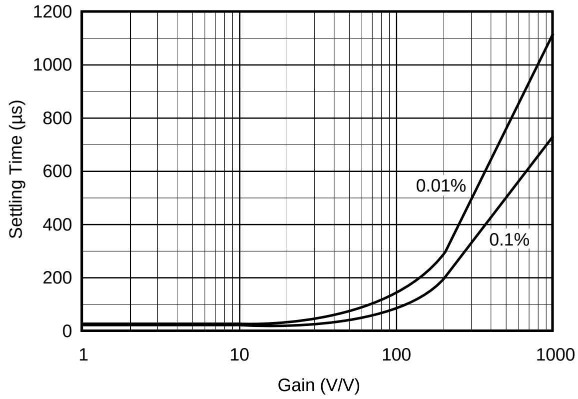



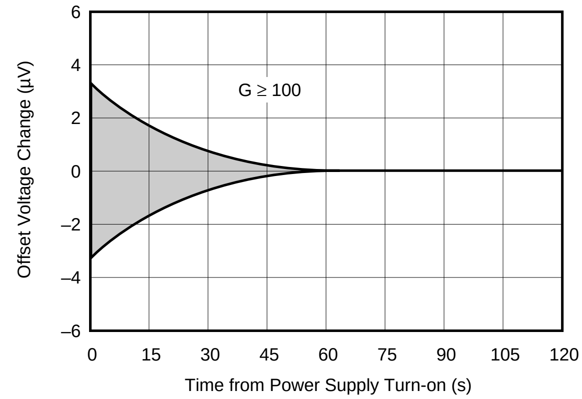
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A$ = +25°C, $V_S$ = ±15V, unless otherwise noted.

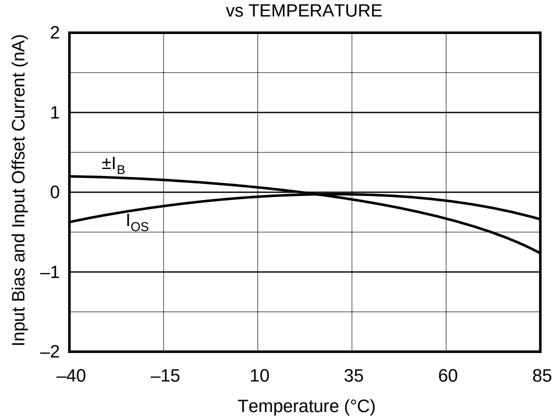
SETTLING TIME vs GAIN



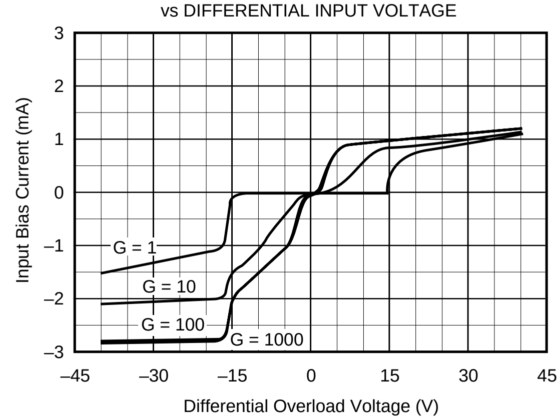

OFFSET VOLTAGE WARM-UP vs TIME



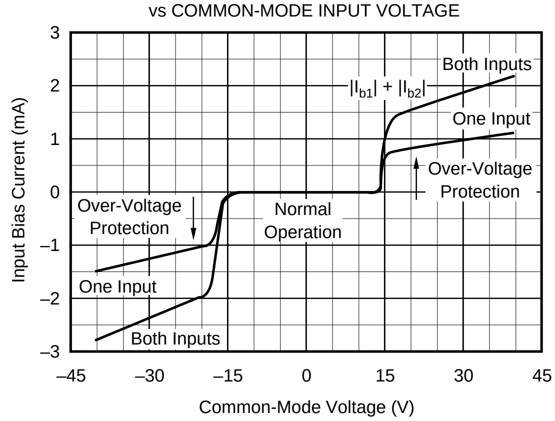

INPUT BIAS AND INPUT OFFSET CURRENT
vs TEMPERATURE



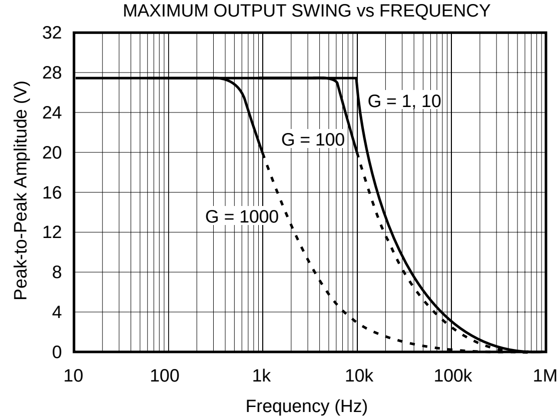

INPUT BIAS CURRENT
vs DIFFERENTIAL INPUT VOLTAGE




INPUT BIAS CURRENT
vs COMMON-MODE INPUT VOLTAGE

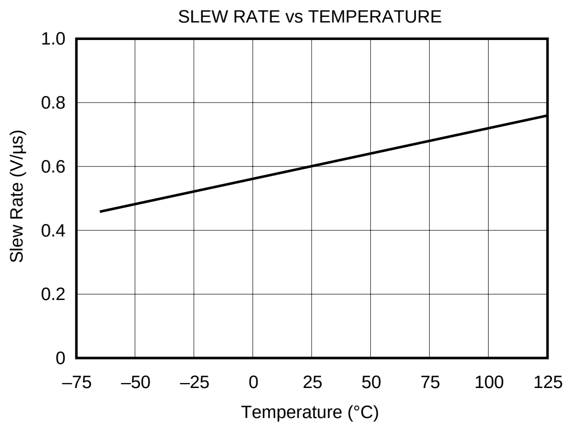


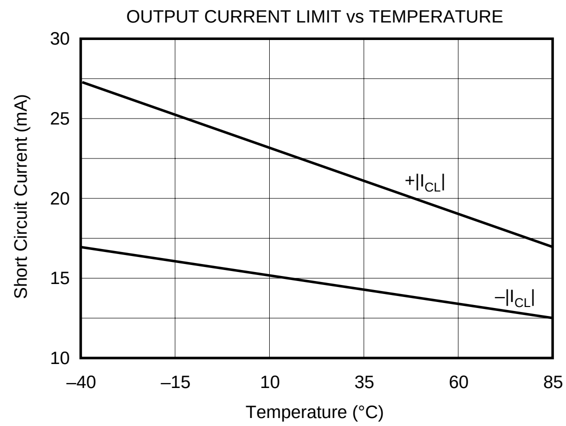

MAXIMUM OUTPUT SWING vs FREQUENCY

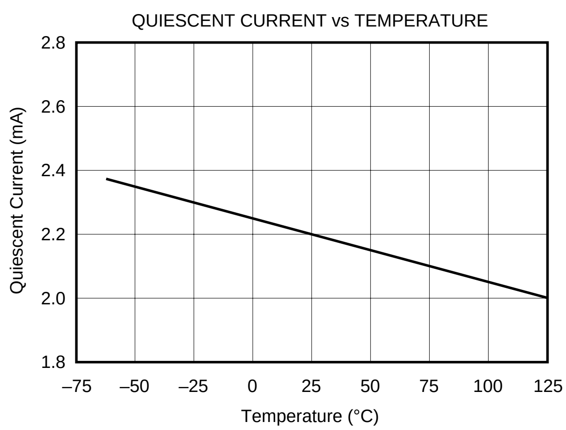


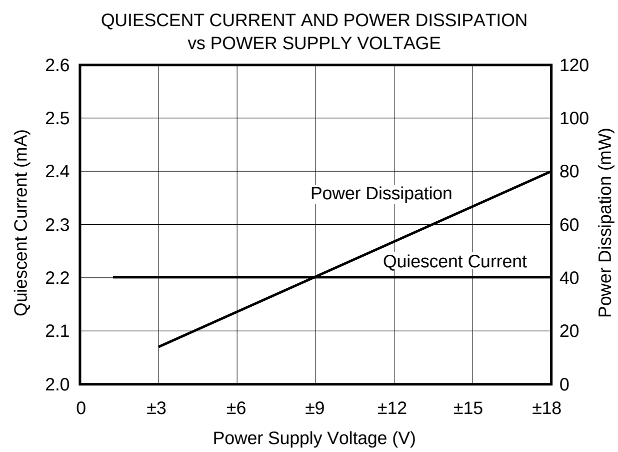
# TYPICAL PERFORMANCE CURVES (CONT)

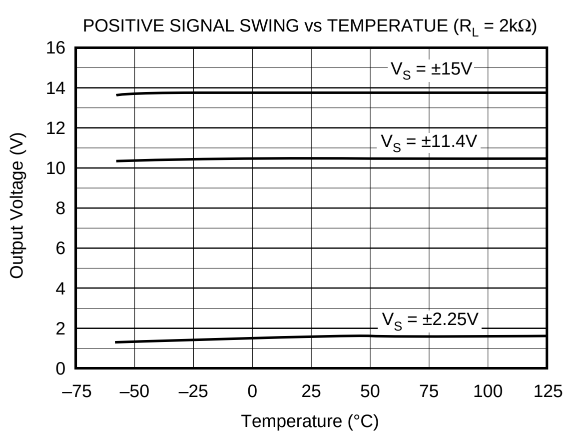
At $T_A = +25°C$, $V_S = ±15V$, unless otherwise noted.

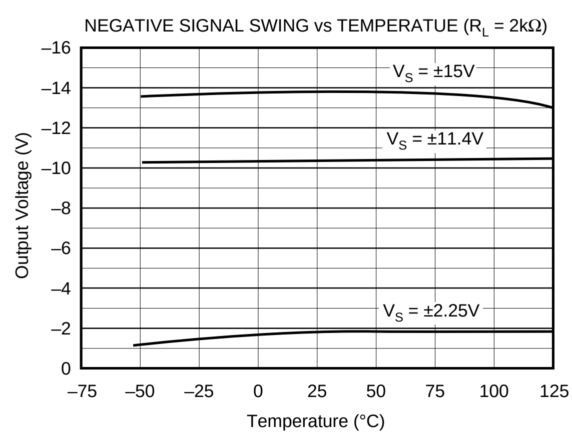


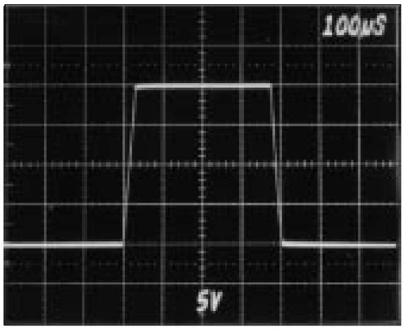



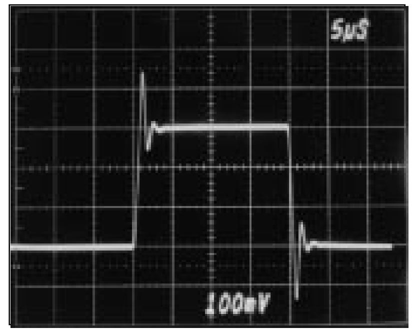
# TYPICAL PERFORMANCE CURVES (CONT)

At $T_A = +25°C$, $V_S = ±15V$, unless otherwise noted.

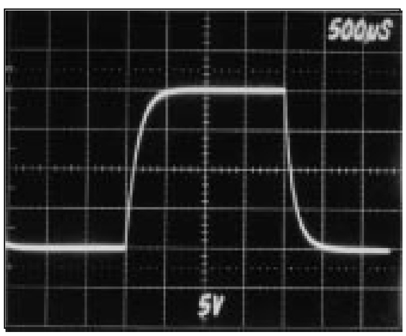
LARGE SIGNAL RESPONSE, G = 1



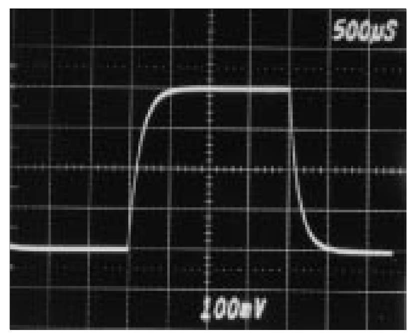

SMALL SIGNAL RESPONSE, G = 1



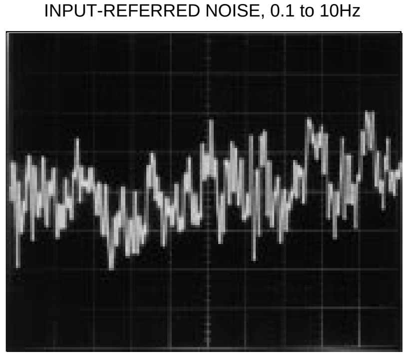

LARGE SIGNAL RESPONSE, G = 1000




SMALL SIGNAL RESPONSE, G = 1000




INPUT-REFERRED NOISE, 0.1 to 10Hz



# APPLICATION INFORMATION

Figure 1 shows the basic connections required for operation of the INA114. Applications with noisy or high impedance power supplies may require decoupling capacitors close to the device pins as shown.

The output is referred to the output reference (Ref) terminal which is normally grounded. This must be a low-impedance connection to assure good common-mode rejection. A resistance of 5Ω in series with the Ref pin will cause a typical device to degrade to approximately 80dB CMR (G = 1).

## SETTING THE GAIN

Gain of the INA114 is set by connecting a single external resistor, $R_G$:

$$G = 1 + \frac{50\ k\Omega}{R_G} \tag{1}$$

Commonly used gains and resistor values are shown in Figure 1.

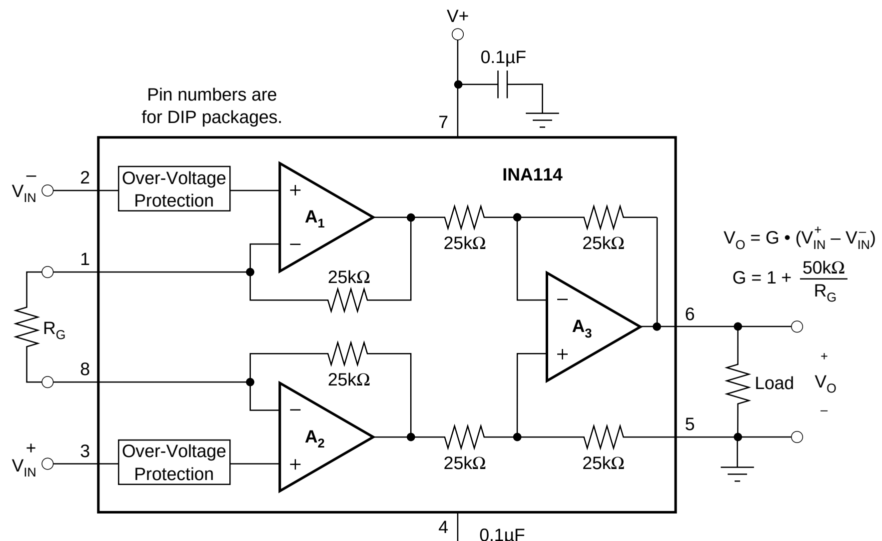
The 50kΩ term in equation (1) comes from the sum of the two internal feedback resistors. These are on-chip metal film resistors which are laser trimmed to accurate absolute values. The accuracy and temperature coefficient of these resistors are included in the gain accuracy and drift specifications of the INA114.

The stability and temperature drift of the external gain setting resistor, $R_G$, also affects gain. $R_G$'s contribution to gain accuracy and drift can be directly inferred from the gain equation (1). Low resistor values required for high gain can make wiring resistance important. Sockets add to the wiring resistance which will contribute additional gain error (possibly an unstable gain error) in gains of approximately 100 or greater.

## NOISE PERFORMANCE

The INA114 provides very low noise in most applications. For differential source impedances less than 1kΩ, the INA103 may provide lower noise. For source impedances greater than 50kΩ, the INA111 FET-input instrumentation amplifier may provide lower noise.

Low frequency noise of the INA114 is approximately 0.4µVp-p measured from 0.1 to 10Hz. This is approximately one-tenth the noise of "low noise" chopper-stabilized amplifiers.




| DESIRED GAIN | $R_G$ (Ω) | NEAREST 1% $R_G$ (Ω) |
|---|---|---|
| 1 | No Connection | No Connection |
| 2 | 50.00k | 49.9k |
| 5 | 12.50k | 12.4k |
| 10 | 5.556k | 5.62k |
| 20 | 2.632k | 2.61k |
| 50 | 1.02k | 1.02k |
| 100 | 505.1 | 511 |
| 200 | 251.3 | 249 |
| 500 | 100.2 | 100 |
| 1000 | 50.05 | 49.9 |
| 2000 | 25.01 | 24.9 |
| 5000 | 10.00 | 10 |
| 10000 | 5.001 | 4.99 |

Also drawn in simplified form:

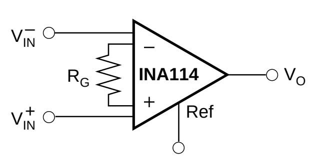



FIGURE 1. Basic Connections.

## OFFSET TRIMMING

The INA114 is laser trimmed for very low offset voltage and drift. Most applications require no external offset adjustment. Figure 2 shows an optional circuit for trimming the output offset voltage. The voltage applied to Ref terminal is summed at the output. Low impedance must be maintained at this node to assure good common-mode rejection. This is achieved by buffering trim voltage with an op amp as shown.

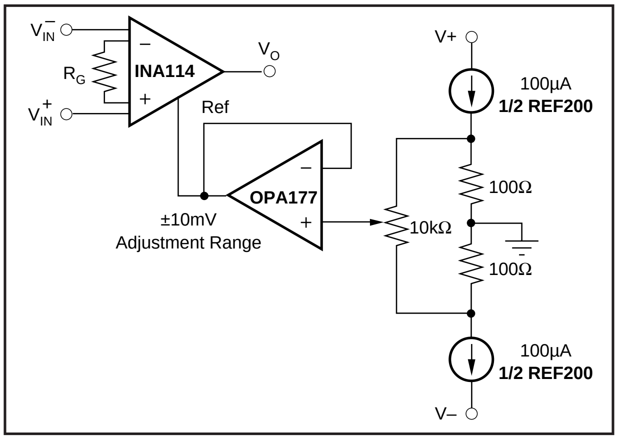



FIGURE 2. Optional Trimming of Output Offset Voltage.

## INPUT BIAS CURRENT RETURN PATH

The input impedance of the INA114 is extremely high—approximately $10^{10}\Omega$. However, a path must be provided for the input bias current of both inputs. This input bias current is typically less than ±1nA (it can be either polarity due to cancellation circuitry). High input impedance means that this input bias current changes very little with varying input voltage.

Input circuitry must provide a path for this input bias current if the INA114 is to operate properly. Figure 3 shows various provisions for an input bias current path. Without a bias current return path, the inputs will float to a potential which exceeds the common-mode range of the INA114 and the input amplifiers will saturate. If the differential source resistance is low, bias current return path can be connected to one input (see thermocouple example in Figure 3). With higher source impedance, using two resistors provides a balanced input with possible advantages of lower input offset voltage due to bias current and better common-mode rejection.

## INPUT COMMON-MODE RANGE

The linear common-mode range of the input op amps of the INA114 is approximately ±13.75V (or 1.25V from the power supplies). As the output voltage increases, however, the linear input range will be limited by the output voltage swing of the input amplifiers, $A_1$ and $A_2$. The common-mode range is related to the output voltage of the complete amplifier—see performance curve "Input Common-Mode Range vs Output Voltage."

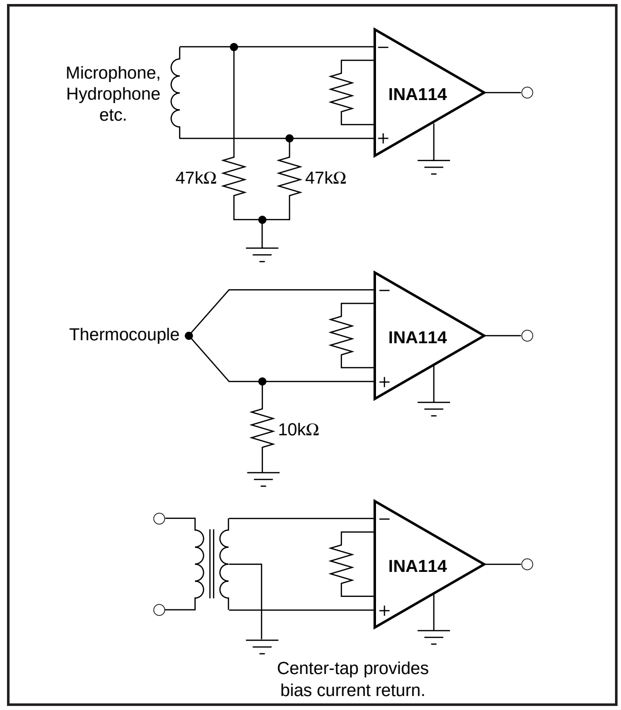



FIGURE 3. Providing an Input Common-Mode Current Path.

A combination of common-mode and differential input signals can cause the output of $A_1$ or $A_2$ to saturate. Figure 4 shows the output voltage swing of $A_1$ and $A_2$ expressed in terms of a common-mode and differential input voltages. Output swing capability of these internal amplifiers is the same as the output amplifier, $A_3$. For applications where input common-mode range must be maximized, limit the output voltage swing by connecting the INA114 in a lower gain (see performance curve "Input Common-Mode Voltage Range vs Output Voltage"). If necessary, add gain after the INA114 to increase the voltage swing.

Input-overload often produces an output voltage that appears normal. For example, an input voltage of +20V on one input and +40V on the other input will obviously exceed the linear common-mode range of both input amplifiers. Since both input amplifiers are saturated to nearly the same output voltage limit, the difference voltage measured by the output amplifier will be near zero. The output of the INA114 will be near 0V even though both inputs are overloaded.

## INPUT PROTECTION

The inputs of the INA114 are individually protected for voltages up to ±40V. For example, a condition of –40V on one input and +40V on the other input will not cause damage. Internal circuitry on each input provides low series impedance under normal signal conditions. To provide equivalent protection, series input resistors would contribute excessive noise. If the input is overloaded, the protection circuitry limits the input current to a safe value (approximately 1.5mA). The typical performance curve "Input Bias Current vs Common-Mode Input Voltage" shows this input current limit behavior. The inputs are protected even if no power supply voltage is present.

### OUTPUT VOLTAGE SENSE (SOL-16 package only)

The surface-mount version of the INA114 has a separate output sense feedback connection (pin 12). Pin 12 must be connected to the output terminal (pin 11) for proper operation. (This connection is made internally on the DIP version of the INA114.)

The output sense connection can be used to sense the output voltage directly at the load for best accuracy. Figure 5 shows how to drive a load through series interconnection resistance. Remotely located feedback paths may cause instability. This can be generally be eliminated with a high frequency feedback path through $C_1$. Heavy loads or long lines can be driven by connecting a buffer inside the feedback path (Figure 6).

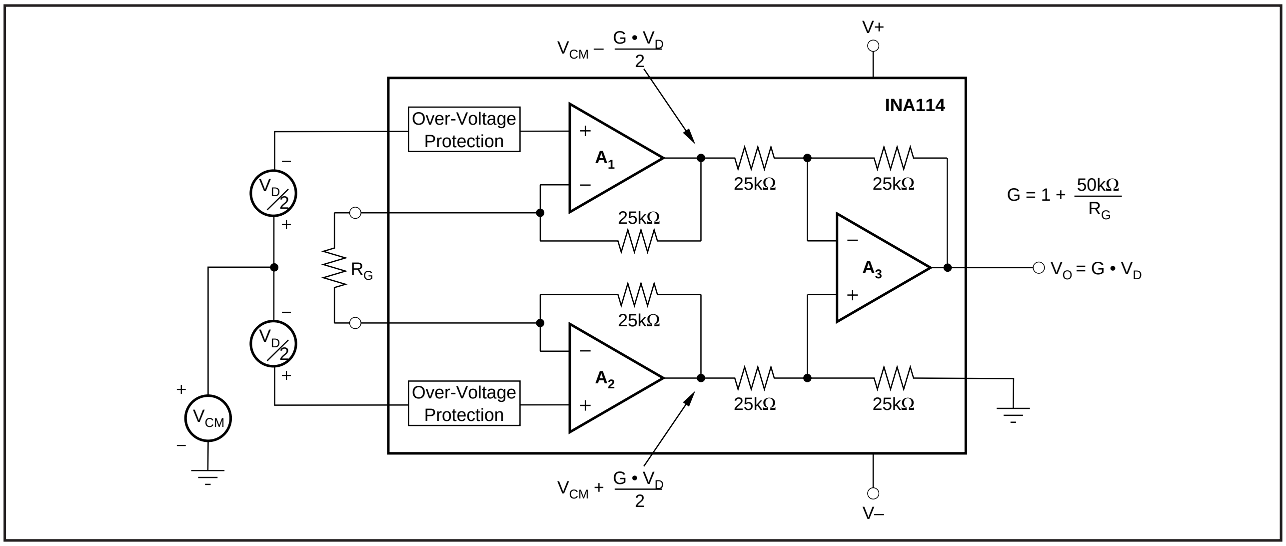



FIGURE 4. Voltage Swing of $A_1$ and $A_2$.

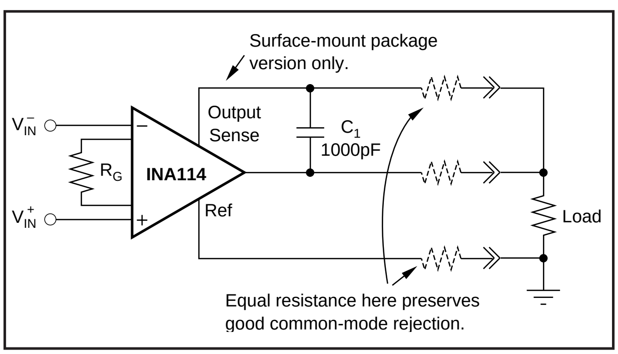



FIGURE 5. Remote Load and Ground Sensing.

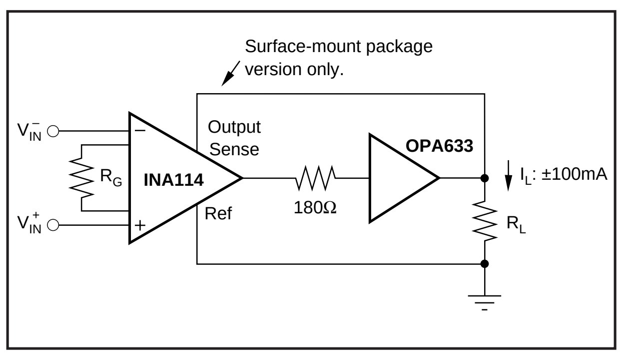



FIGURE 6. Buffered Output for Heavy Loads.

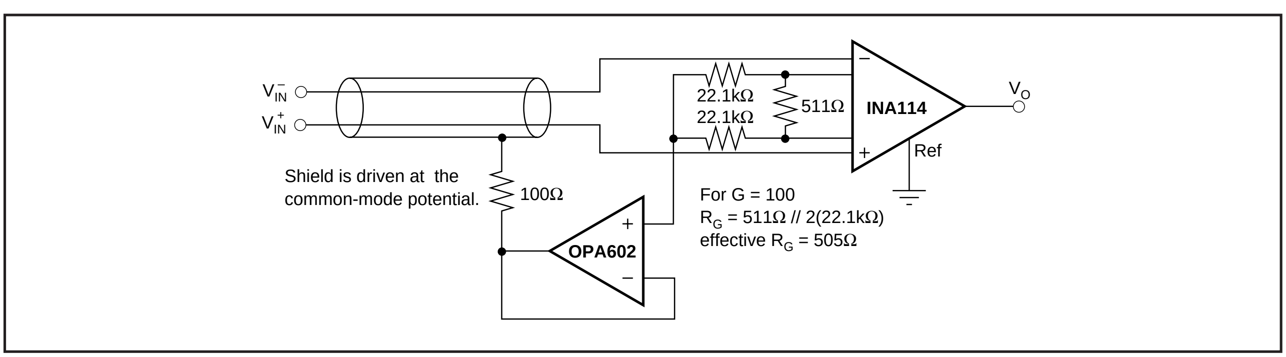



FIGURE 7. Shield Driver Circuit.

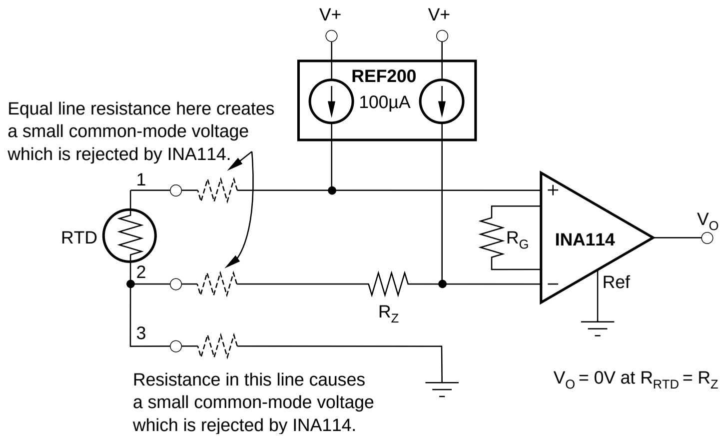
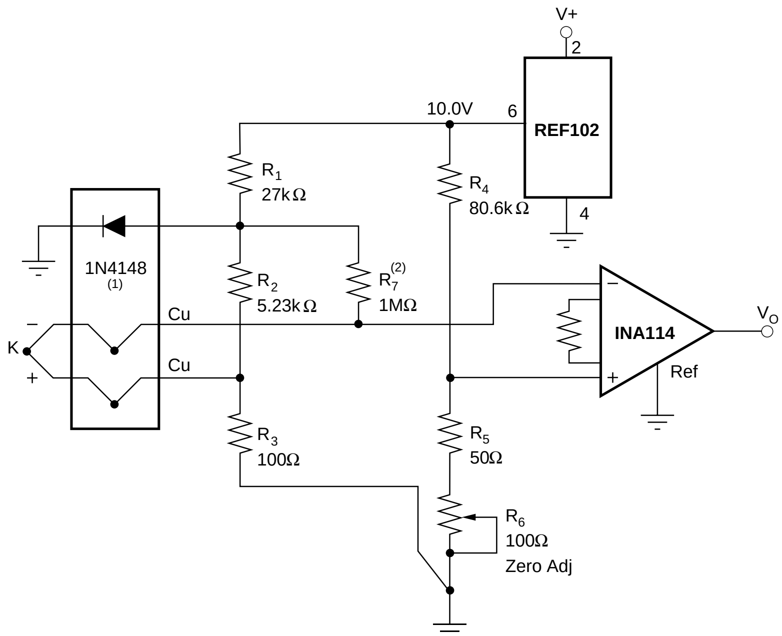



FIGURE 8. RTD Temperature Measurement Circuit.




| ISA TYPE | MATERIAL | SEEBECK COEFFICIENT (µV/°C) | $R_2$ ($R_3$ = 100Ω) | $R_4$ ($R_5$ + $R_6$ = 100Ω) |
|---|---|---|---|---|
| E | Chromel Constantan | 58.5 | 3.48kΩ | 56.2kΩ |
| J | Iron Constantan | 50.2 | 4.12kΩ | 64.9kΩ |
| K | Chromel Alumel | 39.4 | 5.23kΩ | 80.6kΩ |
| T | Copper Constantan | 38.0 | 5.49kΩ | 84.5kΩ |

NOTES: (1) –2.1mV/°C at 200µA. (2) $R_7$ provides down-scale burn-out indication.

FIGURE 9. Thermocouple Amplifier With Cold Junction Compensation.

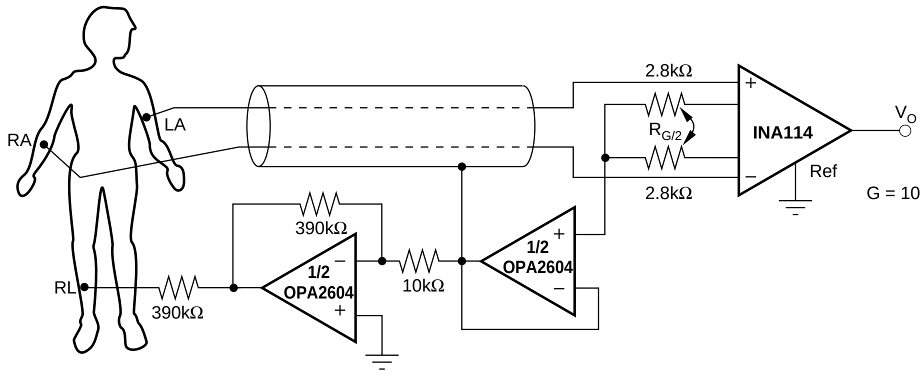



FIGURE 10. ECG Amplifier With Right-Leg Drive.

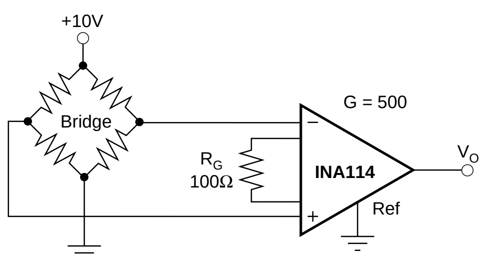



FIGURE 11. Bridge Transducer Amplifier.

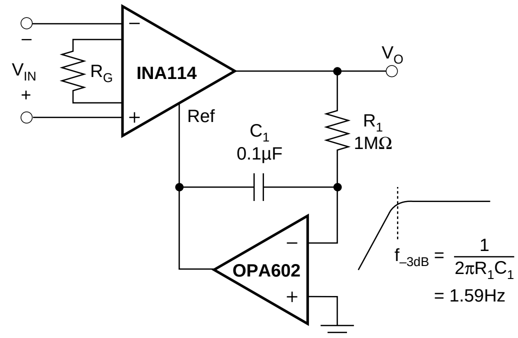
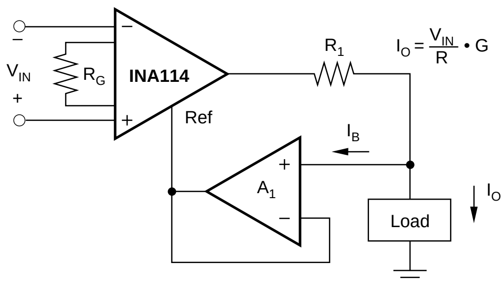



FIGURE 12. AC-Coupled Instrumentation Amplifier.




| $A_1$ | $I_B$ Error |
|---|---|
| OPA177 | ±1.5nA |
| OPA602 | 1pA |
| OPA128 | 75fA |

FIGURE 13. Differential Voltage-to-Current Converter.

## PACKAGING INFORMATION

| Orderable Device | Status [1] | Package Type | Package Drawing | Pins | Package Qty | Eco Plan [2] | Lead/Ball Finish | MSL Peak Temp [3] |
|---|---|---|---|---|---|---|---|---|
| INA114AP | ACTIVE | PDIP | P | 8 | 50 | TBD | CU NIPDAU | N / A for Pkg Type |
| INA114AU | ACTIVE | SOIC | DW | 16 | 48 | Pb-Free (RoHS) | CU NIPDAU | Level-3-260C-168 HR |
| INA114AU/1K | ACTIVE | SOIC | DW | 16 | 1000 | Pb-Free (RoHS) | CU NIPDAU | Level-3-260C-168 HR |
| INA114AU/1KE4 | ACTIVE | SOIC | DW | 16 | 1000 | Pb-Free (RoHS) | CU NIPDAU | Level-3-260C-168 HR |
| INA114AUE4 | ACTIVE | SOIC | DW | 16 | 48 | Pb-Free (RoHS) | CU NIPDAU | Level-3-260C-168 HR |
| INA114BP | ACTIVE | PDIP | P | 8 | 50 | TBD | CU NIPDAU | N / A for Pkg Type |
| INA114BU | ACTIVE | SOIC | DW | 16 | 48 | Pb-Free (RoHS) | CU NIPDAU | Level-3-260C-168 HR |
| INA114BU/1K | ACTIVE | SOIC | DW | 16 | 1000 | Pb-Free (RoHS) | CU NIPDAU | Level-3-260C-168 HR |

[1] The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

[2] Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

[3] MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265